INTEL PENTIUM PRO

MEMBERS:

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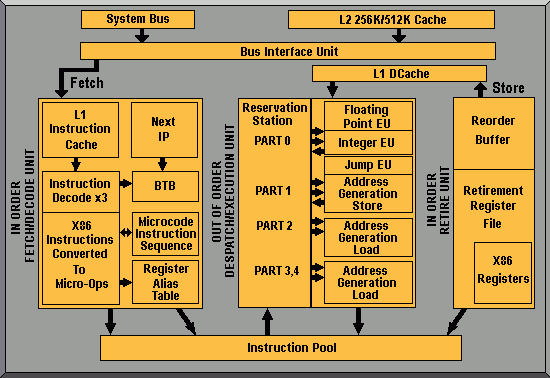
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INTRODUCTION

* Sixth Gen x86 microprocessor, introduced on 1st November 1995.
* Successor of Original Pentium microprocessor.
* Capable of dual and quad –processor configuration.
* 36-bit address bus, supports up to 64 GB Memory.
* It has Error Connection Circuitry, can fix 1-bit and detect 2-bits of error.
* 256 KB or 512 KB L2 cache and 16 KB L1 cache.
* The FSB speeds is between 60 MHz to 66Mhz.
* The Minimum feature size is 0.35 µm to 0.5µm.
* The Most important change in this processor was the use of dynamic execution instead of the superscalar architecture.
* Pipeline is divided in 3 sections Fetch and decode unit, dispatch and execution unit and retire unit.
* Intel Pentium takes CISC instructions and converts them into RISC micro-operations.

INTERNAL STRUCTURE OF PENTIUM PRO



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* The System Bus connects to L2 cache
* BIU controls system bus access via L2 cache.
* L2 cache is integrated in Intel Pentium Pro.
* BIU generate control signals and memory address.
* BIU fetches or passes data or instruction via L1 cache.
* The IFDU can decode three instructions simultaneously and passes it to instruction pool.
* The IFDU has branch prediction logic.
* The DEU then executes the instructions.
* DEU contains three execution units. Two for processing integer instruction and one for processing floating point instruction simultaneously.
* Lastly RU checks the instruction pool and removes decoded instructions that have been executed.
* RU can remove three decoded instructions per clock pulse.

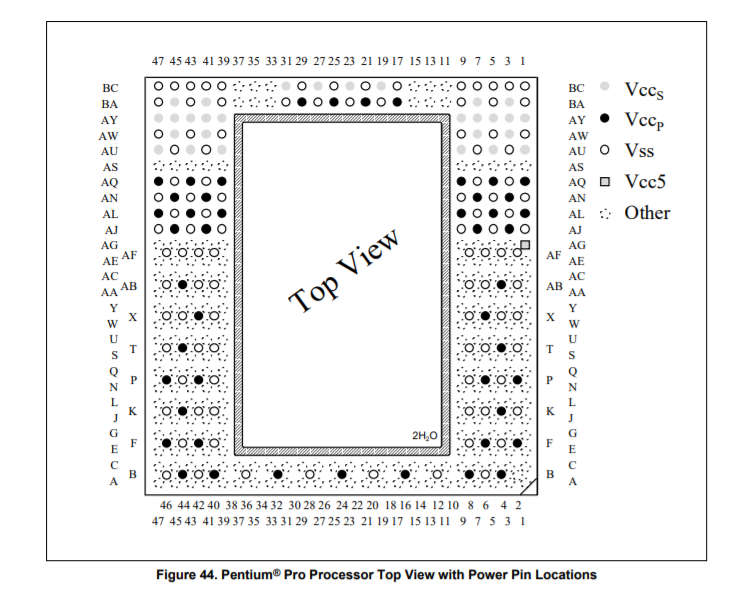
Dynamic Execution

* Intel Pro microprocessor can anticipate jumps in the flow of instructions.
* While the program is being executed processor looks at the instructions further ahead in the program and decides in which order to execute the instructions.
* If The instructions can be executed independently it will execute these instructions in the optimal order rather than in the original program order.

The Memory System

* The Pentium Pro uses a 64-bit data bus to address memory organized in eight banks each contain 8G bytes of data.
* Pentium Pro also has a built in error-correction-circuit. For that the memory system must have room for extra 8-bit number that is stored with each 64 bit number.
* These 8 bit numbers are used to store an error-correction code that allows the Pentium Pro to auto correct any single-bit error.
* An 1M X 72 is an SDRAM with ECC support whereas 1M X 64 is an SDRAM without ECC.

Pentium Pro Pin Diagram



I/O SYSTEM

* Input-output system of Intel Pentium Pro is completely portable with earlier Intel microprocessors.
* A15-A3 address lines with bank enable signals are used to select actual memory banks used for I/O transfer.

DRAWBACK OF INTEL PENTIUM PRO MICROPROCESSOR

* As Intel Pentium Pro uses RISC approach the first drawback is converting instructions from CISC to RISC. It takes time to do so. So, Pentium Pro inevitably takes performance hit when processing instructions.
* Second is that out of order design can be particularly affected by 16-bit code resulting in eventual stop of process.
* ECC scheme causes additional cost of SDRAM that is 72 bits wide.

DIFFERENCE BETWEEN INTEL PENTIUM AND INTEL PENTIUM PRO

* Level-2 cache is integrated in Intel Pentium Pro and not in Pentium microprocessor. This speeds up processing and reduces number of components.
* In Pentium unified cache hold both instructions and data, but in Pentium Pro separate cache is used for instruction and data which speeds up performance.
* Pentium microprocessor doesn’t have jump execution unit or address generation unit as Pentium Pro has, It’s one of the major changes.
* 2M paging isn’t available in Pentium microprocessor. In Pentium Pro 2M paging allows memory above 4G to be accessed.
* Pentium doesn’t have built in error correction circuit, but in Pentium Pro ECC allows correction of one-bit error and detection of two-bit error.

DIFFERENCES BETWEEN INTEL PENTIUM PRO AND INTEL PENTIUM II

* Unlike previous Pentium and Pentium Pro processors, the Pentium II CPU was packaged in a slot-based module rather than a CPU socket.
* Intel improved 16-bit code execution performance on the Pentium II, an area in which the Pentium Pro was at a notable handicap.
* The Pentium II featured 32 KB of L1 cache, double that of the Pentium Pro, as well as deeper write buffers for a slight L1 performance increase.
* The Pentium II was basically a more consumer-oriented version of the Pentium Pro. It was cheaper to manufacture because of the separate, slower L2 cache memory.

DIFFERENCE BETWEEN INTEL 8086 AND INTEL PENTIUM PRO

* In Intel 8086 data bus is 16 bits, whereas in Intel Pentium Pro data bus is 64 bits. Bigger data is equivalent to more processing of data at a given time.
* Again in Intel 8086 address bus is 20 bits whereas in Intel Pentium Pro address bus is 36 bits. Bigger address bus means to communicate with the memory with more data at a given time.
* 8086 operates on 5V and Pentium Pro requires a single +3.3V or +2.7V to operate.

Conclusion:

The Pentium Pro processor was designed to achieve significantly higher performance than the Pentium processor in the same process technology. It achieves this performance through a super pipelined design that yields a 25% faster clock, and with an out of order dynamic execution engine that reduces the CPI. The data presented here shows that the Pentium Pro processor achieves a 15 to 45% reduction in CPI compared to the previous generation design (Pentium processor) in the same process technology, while running at a 25% faster clock frequency. The processor’s out-of-order, speculative execution engine does manage to overlap useful work with pending memory accesses to reduce the impact of cache misses. The impact of resource stalls is also reduced by out of order execution. The branch prediction scheme reduces branch mispredictions so as not to make them a significant performance limiter. It performs well even on old binaries that were not optimized for its microarchitecture. Performance counter-based measurements show that the overall CPI achieved by the Pentium Pro processor is about 20 to 50% lower than the individual latency components due to overlapped execution.